III. REMARKS

Claims 1-24 and 31-36 are pending in this action. By this amendment, claims 25-30 have been cancelled, and claims 31-36 have been added. Applicants do not acquiesce in the correctness of the rejections and reserve the right to present specific arguments regarding any rejected claims not specifically addressed. Further, Applicants reserve the right to pursue the full scope of the subject matter of the original claims in a subsequent patent application that claims priority to the instant application. Reconsideration in view of the above amendments and following remarks is respectfully requested.

In the Office Action, claims 1-24 are rejected under 35 U.S.C. 102(a) as allegedly being anticipated by Regan (US 6,756,242). Applicants respectfully traverse this rejection for the reasons that follow.

With respect to independent claims 1, 9 and 17, Regan does not disclose each and every claimed feature. For instance, the claimed invention includes, *inter alia*, "determining a scaling factor for each problem object[,]" as recited in claim 1 and claimed similarly in claims 9 and 17. Regan, however, only includes "calculating a plurality of predetermined scaling ratios (of an integrated circuit) and selecting a scaling factor that is equal to or greater than the largest of the predetermined scaling ratios." (Col. 2, lines 26-29, parenthetical explanation added). For example, in Regan, the three factors in the general scaling calculation, i.e., variable geometry values, absolute geometry values and the design grid (*see* col. 5, lines 60-62), are all considered and have to be considered with respect to the whole integrated circuit, not an individual problem object. For example, regarding variable geometry values, Regan requires that "the separation 4, the overlap 5, and the width 6 of different geometries must be equal to or greater than a set dance." (Col. 6, lines 7-9). For another example, regarding a design grid, Regan requires "[a]ll

co-ordinates in the final chip must be place [*sic.*] on the defined design grid." (Col. 6, lines 29-31). In view of the forgoing, in calculating a general scaling ratio, Regan only considers relationships among and between multiple parts (i.e., the whole chip), but not each individual problem object.

In addition, the listed three scaling ratios of Regan, i.e., interconnect scaling ratio, via size ratio and enclosure, and transistor geomctry ratio (*see* col. 6, lines 39-52) are not determined for each individual problem object. For example, "the via size is the size of the fixed rectangles that make up the via holes between routing layers." (Col. 6, lines 45-46, emphasis added). For another example, "[t]he transistor geometry ratio is the relative shrink of the shapes that make up the distance between two transistors in separate pieces of diffusion[.]" (Col. 6, lines 53-55, emphasis added). As such, the predetermined scaling ratios in Regan are not for each individual problem object. In view of the foregoing, Regan does not disclose "determining a scaling factor for each problem object[.]" (Claim 1).

With further regarding to claims 1, 9 and 17, Regan does not disclose, *inter alia,* "determining which at least one of a plurality of scaling techniques is to be applied to each problem object, and scaling each problem object with a respective at least one scaling technique and scaling factor[.]" (Claim 1, similarly claimed in claims 9 and 17). In Regan, "the entire circuit is scaled using the [same] calculated factor[.]" (Col. 4, lines 27-28, addition ours; also see col. 4, lines 28-29.) Moreover, "[r]elative scaling involves multiplying each co-ordinate in the shape by the same scale factor to adjust the co-ordinates." (Col. 11, lines 66-67 of Regan, emphasis added). As such, Regan excludes the possibility of determining and applying a separate scaling technique and scaling factor for each individual problem object. That is, Regan does not determine which at least one of a plurality of scaling techniques is to be applied to each

problem object, and does not scale each problem object with a respective at least one scaling technique and scaling factor.

Although it is mentioned in the background of Regan that "different parts and components of the circuit may need to be scaled by differing factors" (col. 1, lines 29-30), Regan does not disclose features of the claimed invention as, e.g., discussed above. In addition, in making the above statement, Regan still considers only the whole IC chip, but not the identified problem object. (*See* col. 1, lines 27-28, "[t]he overall plan of the circuit may be approximately the same[.]") Moreover, Regan does not disclose/expect a successful implementation of scaling different parts/components with different factors. Instead, Regan itself attempts to use the same scaling ratio for all the parts/components on an IC chip. One reason is that Regan does not possess a method for scaling different parts of an IC by different scaling factors, which is claimed in the co-pending application of the current Applicants (US Patent Application 10/438,625). In view of the foregoing, Regan does not anticipate the claimed invention. Accordingly, Applicants respectfully request withdrawal of the rejection.

The newly added independent claims 31, 33 and 35 include the allowable features of claims 1, 9 and 17, respectively. In addition, claims 31, 33 and 35 include, *inter alia*, "the scaling factor includes at least one of a compensation and a new ground rule." Regan, however, only discloses using a scaling ratio, not a compensation or a new ground rule. No new fees are required for these claims.

Applicants respectfully submit that the application is in condition for allowance. Should the Examiner believe that anything further is necessary to place the application in better condition for allowance, he is requested to contact Applicants' undersigned attorney at the telephone number listed below.

Respectfully submitted,

Spencer K. Warnick
Reg. No. 40,398

Date: 4/19/06

Hoffman, Warnick & D'Alessandro LLC
75 State Street, 14th Floor
Albany, New York 12207
(518) 449-0044
(518) 449-0047 (fax)